Exploring the Inner Workings of Neuron Circuits That Exhibit Persistent Activity To Explain How Working Memory and Executive Function Are Implemented in The Brain

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ABSTRACT

In this research we explore in detail how a phenomenon called "sustained persistent activity" is achieved by circuits of interconnected neurons. Persistent activity is a phenomenon that has been extensively studied (Papoutsi et al. 2013; Kaminski et. al. 2017; McCormick et al. 2003; Rahman, and Berger, 2011). Persistent activity consists in neuron circuits whose spiking activity remains even after the initial stimuli are removed. Persistent activity has been found in the prefrontal cortex (PFC) and has been correlated to working memory and decision making (Clayton E. Curtis and Daeyeol Lee, 2010).

We go beyond the explanation of how persistent activity happens and show how arrangements of those basic circuits encode and store data and are used to perform more elaborated tasks and computations.

The purpose of the model we propose here is to describe the minimum number of neurons and their interconnections required to explain persistent activity and how this phenomenon is actually a fast storage mechanism required for implementing working memory, task processing and decision making.

INTRODUCTION

In this research we explore the existence of neuron circuits in the brain that store information in a way that has not been well understood. It is known that memories are kept in the brain in the synapses of large collections of neurons (Mayford et al. 2012). These synapses are dynamically modified through learning processes and adaptation. Synaptic plasticity is accomplished by two opposite processes: long-term potentiation (LTP) and long-term depression (LTP). Changing the strength of a synapse by means of LTP or LDP takes between 10 and 30 minutes in average (Wang X. et al. 2015; Rosenberg et al. 2016; Le Duigou et al. 2015; De Pasquale et al. 2014; Wang Hui et al. 2016).

To perform intermediate calculations in a timely manner, we hypothesize that the brain also keeps memories on neuron arrangements like the one proposed in this research article. The information stored on such circuits store information as sustained bursts of action potentials that

can be activated (set) or deactivated (reset) on demand, thus, storing one bit of information at speeds several orders of magnitude faster than the long-term memories stored on synapses. The brain needs to react quickly to external stimuli and to do so we argue that neuron flip-flops are used to provide this type of immediate temporary memory. We introduce the term Neuron Flip-Flop which is a circuit made of three neurons connected in such way that persistent activity is achieved. We name these circuits neuron flip-flops (NFF) for their similarity to equivalent devices in the computer engineering world (Gupta and Mehra, 2016). Neuron flip-flops also facilitate sequential processing which is a way to execute algorithms in the brain. Neuron flip-flops hold intermediate states during a multi-step task. Those states can be interrogated and decision making is made by evaluating the current state of a neuron flip-flop (NFF).

These neuron circuits (NFF) have been found in the prefrontal cortex (PFC) (Compte Albert, 2006; Fellous et al. 2003) and could also be probably found in the CA1 or CA3 nuclei of the hippocampus where endogenous oscillations have been found (Jochems et al. 2013; Pinsky et al. 1994; Xu et al. 2008), the hippocampus entorhinal cortex (EC) and amygdala (Egorov et al., 2006) and very likely on the dentate gyrus (DG) which has neurons whose spiking pattern is of type NASP (Non-Adapting Spiking) as classified by the Hippocampome project (Komendantov et al. 2019; Hippocampome). These DG neurons exhibit the closest spiking pattern matching the results of our simulations.

It is worth mentioning that oscillations (bursts of spikes) are present in the brain and have been studied extensively. As an example, pyramidal CA3 neurons in the hippocampus exhibit endogenous bursts of spikes whose frequency has been found to be associated with the intensity of the stimuli (Balind et al. 2019; Harris et al. 2001). Theta oscillations are widely found in the hippocampus and associated to several functions. For example, neocortical neurons are significantly phase-locked to hippocampal theta oscillations during either spatial exploration or REM sleep (Sirota et. al. 2008). Theta oscillations are most regular in frequency and largest amplitude in the stratum lacunosum-moleculare of the hippocampal CA1 region and are also present in the dentate gyrus and the CA3 region (Buzsa 2002). Theta oscillations have also been found in the amygdala (Paré D et al. 2000) and in the entorhinal cortex (Alonso A. et al. 1987).

Based on our hypothesis that a different memory storage mechanism must exist in the brain, we devised a model that has three neurons interconnected in such way that can store one bit of information without resorting to the plasticity of their synapses. What this circuit stores is an oscillation (a burst of action potentials) and the oscillate or do-not-oscillate state is controlled on demand.

The neuron circuit proposed in this research is made of three neurons that do not necessarily exhibit endogenous bursting features as those found in CA3 pyramidal neurons.

The circuit, named Set-Reset Neuron Flip-Flop (SR NFF), has two independent inputs (a Set signal and a Reset signal) and one output, the Q signal that represents the value stored on the circuit.

Figure 1 shows the SR NFF circuit along with the timing of the input, feedback and output signals. The Set signal is a presynaptic action potential that is applied to a dendrite having an

excitatory synapse on input neuron X0. The arrival of an impulse on this input dendrite will drive all three neurons in a sustained spiking state that remains oscillating even after the stimulus is removed, thus storing a value on the circuit (bursting).

Output neuron (Q) is not required for the persistent activity (sustained spiking) but it is necessary to deliver the value of the device to other neuron circuits. Neuron Q must have dozens or even hundreds of axon terminals and must be capable of sending neurotransmitters to them at a fast pace. Neurons X0 and X1 on the other hand, only need an axon with a single axon terminal and one axonal branch.

The oscillation is carried out by the positive feedback connection between middle neuron X1 axon and the feedback dendrite of input neuron X0. This feedback dendrite has an excitatory synapse with axon X1 terminal. Figure 4 shows the sequence of events; once the input stimulus makes neuron X0 fire, an action potential travels on axon X0 to input dendrite of middle neuron X1, which arrives at the soma of neuron X1 which in turn fires an action potential on its axon. As the action potential on axon X0 dies, an action potential from X1 arrives at its feedback dendrite resulting in neuron X0 fire a new action potential. The cycle is repeated indefinitely until an action potential arrives at Reset dendrite of input neuron X0. The reset dendrite has an inhibitory synapse that causes hyperporalization of the soma of X0.

The spiking / no spiking state of the circuit effectively stores one bit of information. It is important to emphasize that the input stimuli can be removed and the circuit will stay in the state determined by the nature of the stimulus (Set/Reset).

The output neuron Q relays the sustained bursting to its axon which is the output of the circuit. One axonal branch of axon X1 with an excitatory synapse on a dendrite of neuron Q transmits the signal from X1 to Q.

The period of the oscillation is the sum of time delays due to the geometry of dendrites and axons (length and diameter), impedances, capacitances, and synapses delays. There are not specific required parameters to have this circuit behave in this way. Several other configurations are possible, such as all signals -Set, Reset and Feedback- connected to a single dendrite on neuron X0, or even axo-somatic or axo-axonic synapses as well.

To test the circuit's physiological ability to function as proposed, a model was developed using software tool Neuron© by Yale University. The model and its results are explained in the next section.

SIMULATION OF A SINGLE NEURON FLIP-FLOP

Software tool Neuron© by Yale University (Carnevale, N.T. and Hines, M.L 2006) was used to create a model according to Figure 1. The parameters for all somata, dendrites and axons were defined with the default values Neuron© provides. Only dendrite and axon lengths were specified and synapses were tuned to exhibit the required inhibitory or excitatory feature as well as time delays.

The resulting data was exported to external files and MATLAB® was used to read the files and generate the figures presented below.

To simulate the Set and Reset signals, current clamps were used at different times. The currents are injected on input neuron X0 respective dendrites. The length of the experiment was 500 ms. Figure 2 shows an excitatory current applied to neuron X0 Set dendrite at times 10 ms and 350 ms, and an inhibitory current applied at times 250 ms and 400 ms on Reset dendrite. The spiking voltage of axon X0 is shown immediately after the Set signal is applied. Axon X0 stops spiking and stays at rest potential (polarized) as expected after a Reset signal is injected.

Figure 3 shows the action potentials of all axons along the 500 ms. There is an inherent delay between the spikes of the three neurons due to the propagation delay down the dendrites, axons and synapses. This delay is shown in more detail on Figure 4, which shows the first 45 ms of the experiment only.

NEURON FLIP-FLOPS AT WORK (WORKING MEMORY)

Working Memory refers to our ability to temporarily maintain and process information (Masse, Song et al. 2019), (Izaki et al., 2008). Having elucidated the inner workings of a circuit that exhibits sustained persistent activity and showing that effectively, this circuit stores one bit of information, we continue to show how arrays of several NFF wired appropriately implement more complex circuits that perform working memory tasks.

We have chosen a simple task we are all familiar with: perform the arithmetic sum of two one-digit numbers. Figure 5 shows schematically the components of a circuit that computes R = A + B where A and B are one digit numbers, from 0 to 9.

On the left side of the figure the two operands, A and B, are shown as registers (arrays of neuron flip flops). Each number is represented as one-and-only-one flip-flop on its ON state (persistent activity) at a given time. In this example, the objective is to obtain the sum 4+3, and thus, on register (operand) A, its flip-flop # 4 is set by applying an action potential on its Set input. Similarly, for register (operand) B, its flip-flop # 3 is set by applying an action potential on its Set input. The result of the sum, 7, is obtained by means of an inter network of neurons that are wired to perform the sum (what we know as the sum fact table). This inter network has 10 outputs, one for each possible result (0-9) which delivers by appropriately sending an action potential to the appropriate Set input of the Result register.

The adder circuit was modeled and simulated with Neuron© with the values shown on Figure 5, Z = 4 + 3. On Figure 6, the values of all 10 bits of operand A are shown. Only flip-flop #4 exhibits persistent activity while others are at their resting (polarized) potential. Similarly on Figure 7, operand B value is shown, with flip-flop #3 spiking while all others are polarized.
Similarly, on Figure 8, the value of the result, register Z, is shown: only flip-flop #7 exhibits sustained persistent activity.

Even a simple task as adding two one digit numbers, requires a series of steps, which are

numbered in circles on Figure 5. These are the steps:

1. Reset (erase) all neuron flip-flops of registers (operands) A and B by applying an action potential to all the Reset inputs of all flip-flops

2. Load value of operand A: Apply an action potential to the Set input of the appropriate flip-flop of Register A.

3. Load value of operand B: Apply an action potential to the Set input of the appropriate flip-flop of Register B.

4. Reset (erase) all neuron flip-flops of register Result

5. Compute. This is an action potential that sets a flip-flop that is connected in a logical AND way which each of the 10 output lines of the Inter Neuron Network. Only one is transferred to the appropriate Set input of register Result, thus, yielding the sum of A and B.

Now, the next obvious question and a very important one is, how the brain implements sequence?

The answer is again, a variation of the neuron flip-flop (NFF) called a monostable (as they are known in the computer engineering world) (Chien Hung-Chun and Lo Yu-Kang, 2011). These are circuits that hold one bit of information for some predefined time and reset themselves after the time is up. The following section explains in more detailed the circuits that implement task sequencing in the brain.

EXECUTIVE FUNCTION: TASK SEQUENCING

We argue that neuron flip-flops are the fundamental circuits (devices) in the brain that implement fast temporary storage (working memory) and also, with some additional interconnections, provide the function of task sequencing, necessary to perform conscious tasks that require several steps executed in sequence.

On Figure 9 we show the basic monostable circuit, which consists of a neuron flip-flop with a delay line connected from its output, Q, to its own reset input. A delay line is simply implemented by several neurons connected in daisy chain. The time required for an action potential to arrive at the reset input, is the delay of the monostable. This circuit, once an action potential is applied to its Set input, begins spiking on its output axon Q, exhibiting persistent activity. However, the output axon Q, has a synapse with a neuron which in turn has its axon connected to another neuron's dendrite, perhaps several neurons in cascade, in such way that they implement a delay line that has its last axon connected to the Reset input of the neuron flip-flop. That way, after some time determined by the number of neurons on the delay line and their physical characteristics, the neuron flip-flop resets itself.

By connecting several monostables in sequence as shown on Figure 10, a task sequencer is effectively implemented. The output axon action potential of each stage is used to activate

another neural circuit that performs a particular task, thus, a task sequencer circuit executes several steps sequentially.

The circuit was simulated with Neuron© and the resulting signals are shown on Figure 11.

CONCLUSION AND FUTURE WORK

The brain needs to perform computations that require fast, intermediate storage that cannot be implemented on slow adapting synapses. Additionally, the brain executes complex executive function tasks in sequences of several steps. We hypothesize that all these functions are based on a well known phenomenon called Sustained Persistent Activity. A neuron flip-flop circuit that stores one bit of information has been proposed, modeled, simulated and the results are found to align with the expectations. Arrays of neuron flip-flops are used by the brain to symbolically represent data and arrangements of neuron flip-flops are used to implement task sequencing.

Future research will continue to determine how other critical functions take place in the brain, namely, how comparing two values is accomplished; how the result of a comparison is used to branch to another step in a task sequence; how data is moved between arrays of neuron flip-flops and between arrays of NFFs and other neural networks on the neocortex and other areas, which hold memories on their synapses.

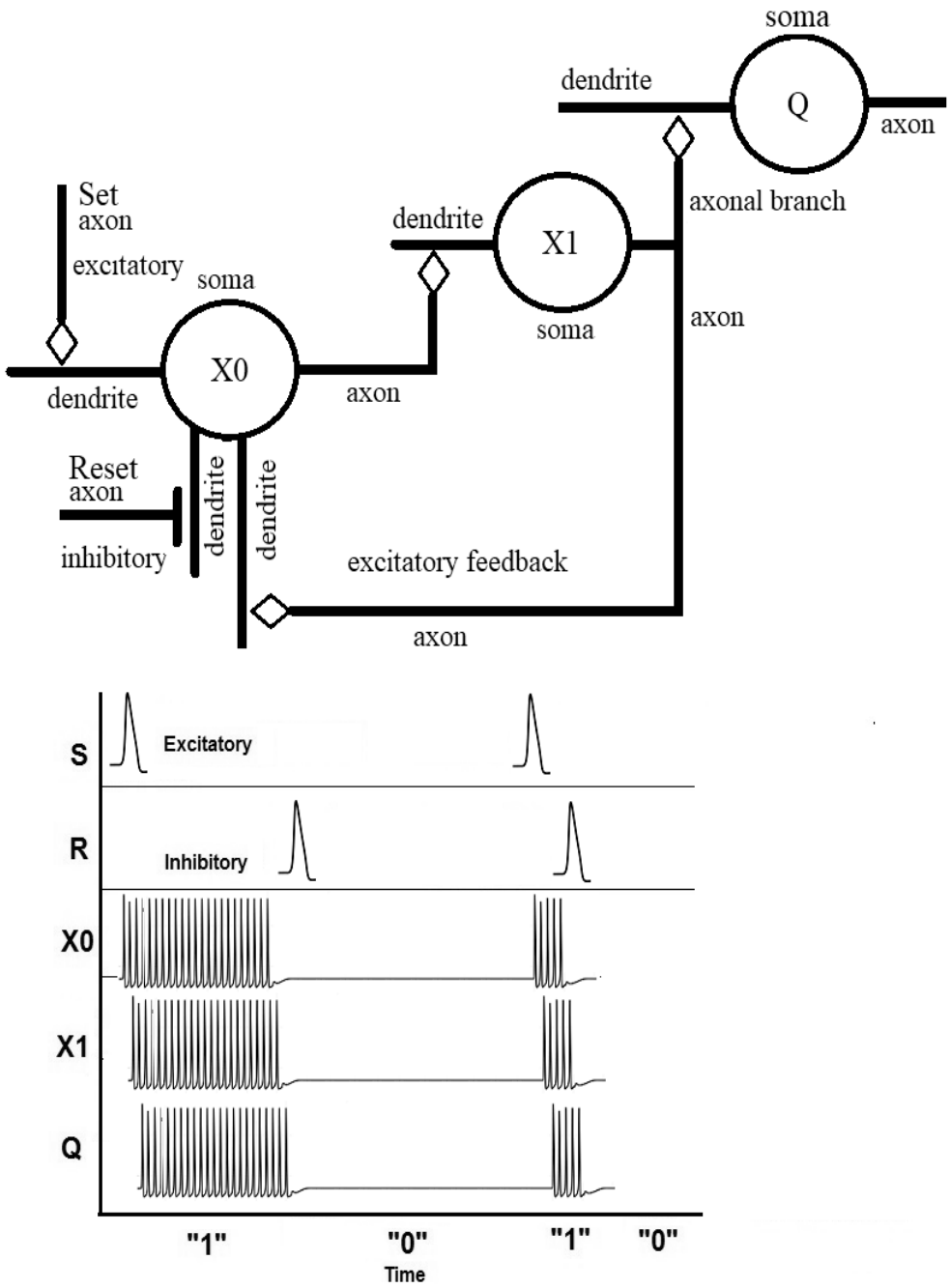

Figure 1. A Neuron Set-Reset Flip-Flop

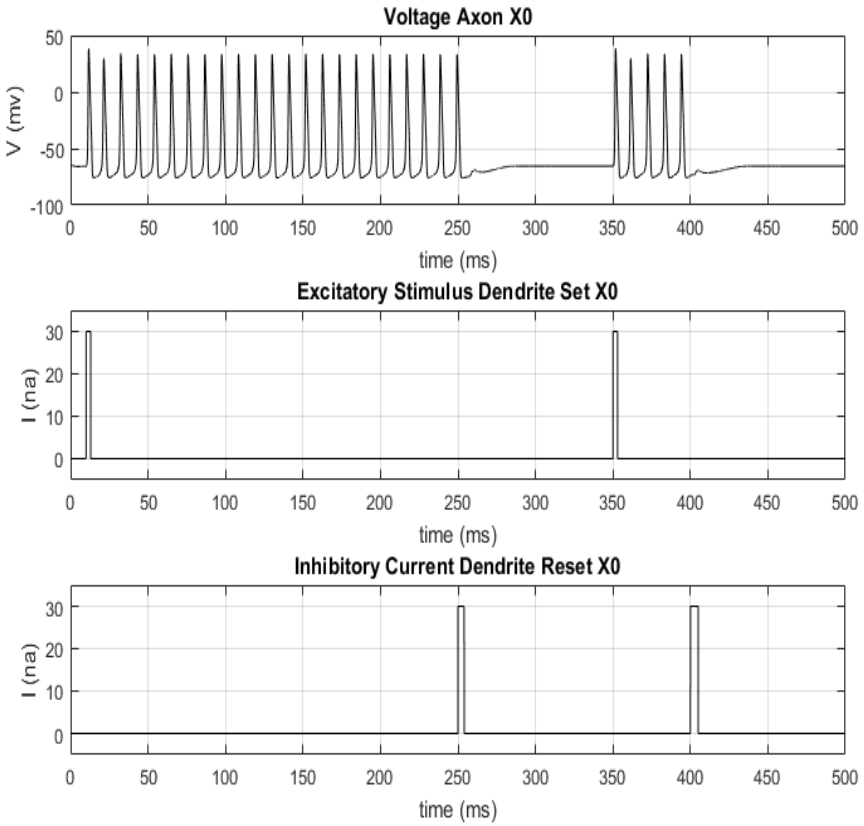

Figure 2. Axon X0 voltage relative to excitatory (Set) and inhibitory (Reset) signals.

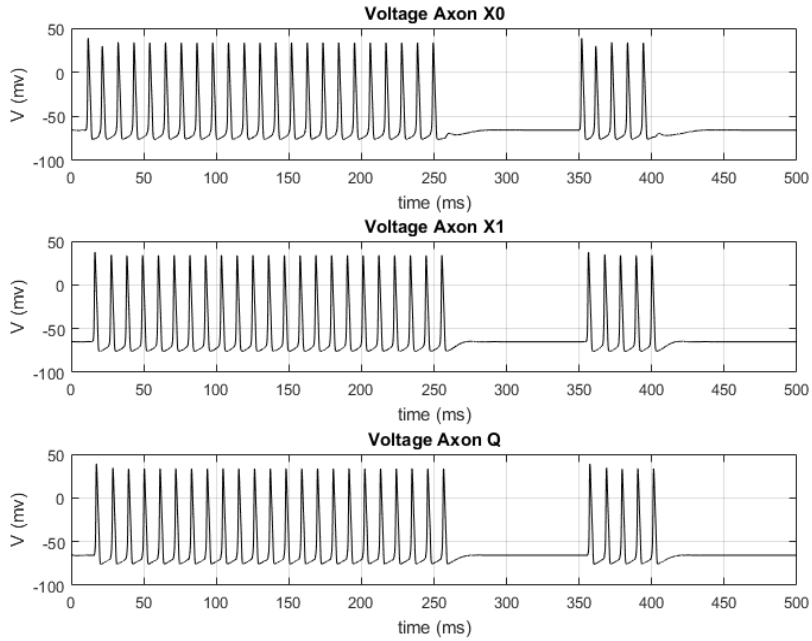

Figure 3. Voltages on all three axons.

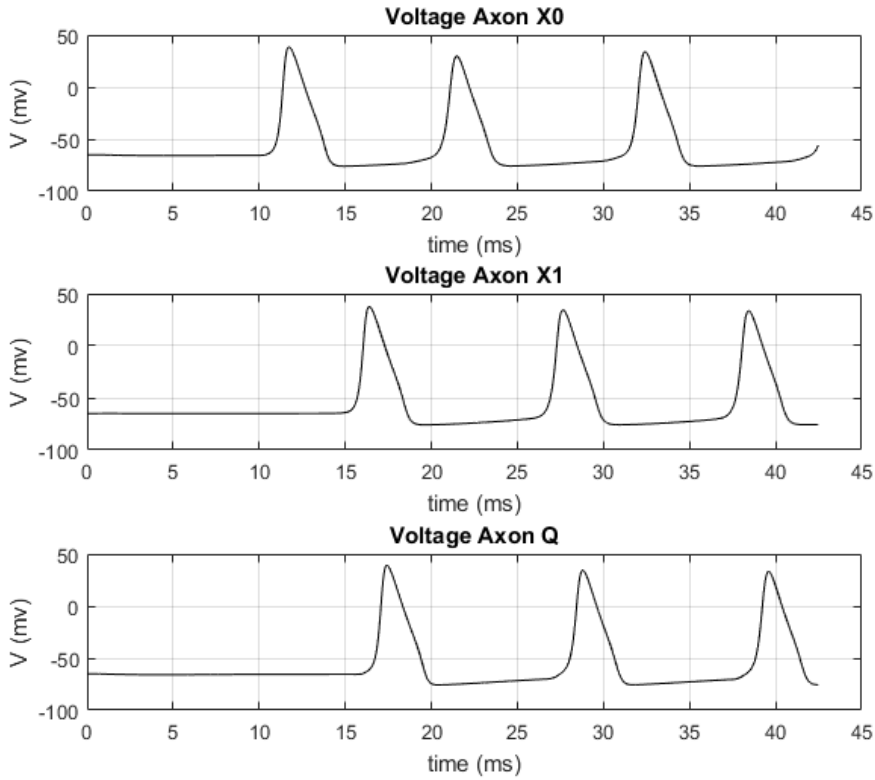

Figure 4. Voltages on all three axons for the first 45 ms showing the delays between them.

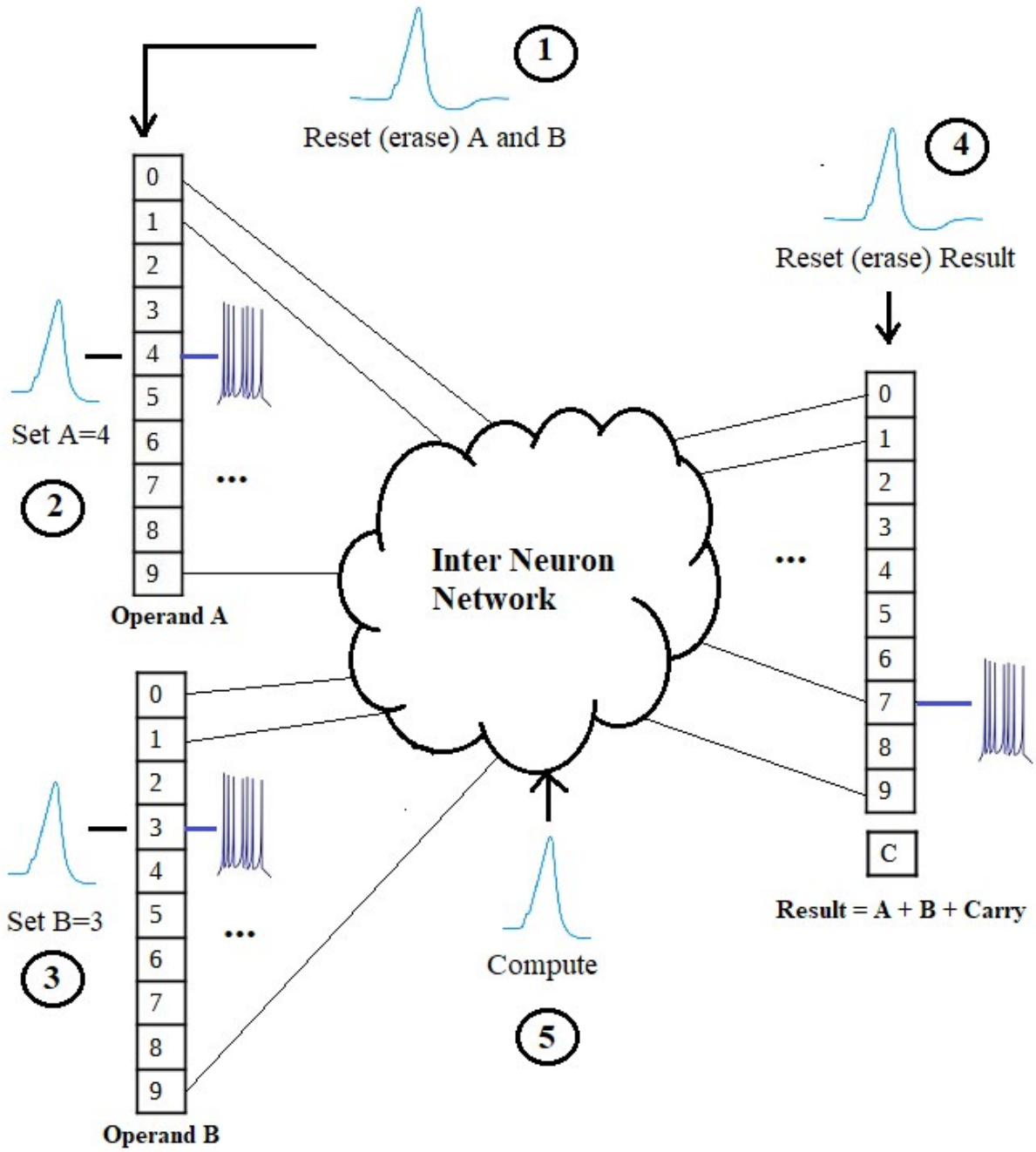

Figure 5. Computation of the sum A+B with 2 registers for the operands and one register for the result. The numbers in circles indicate the sequence of events.

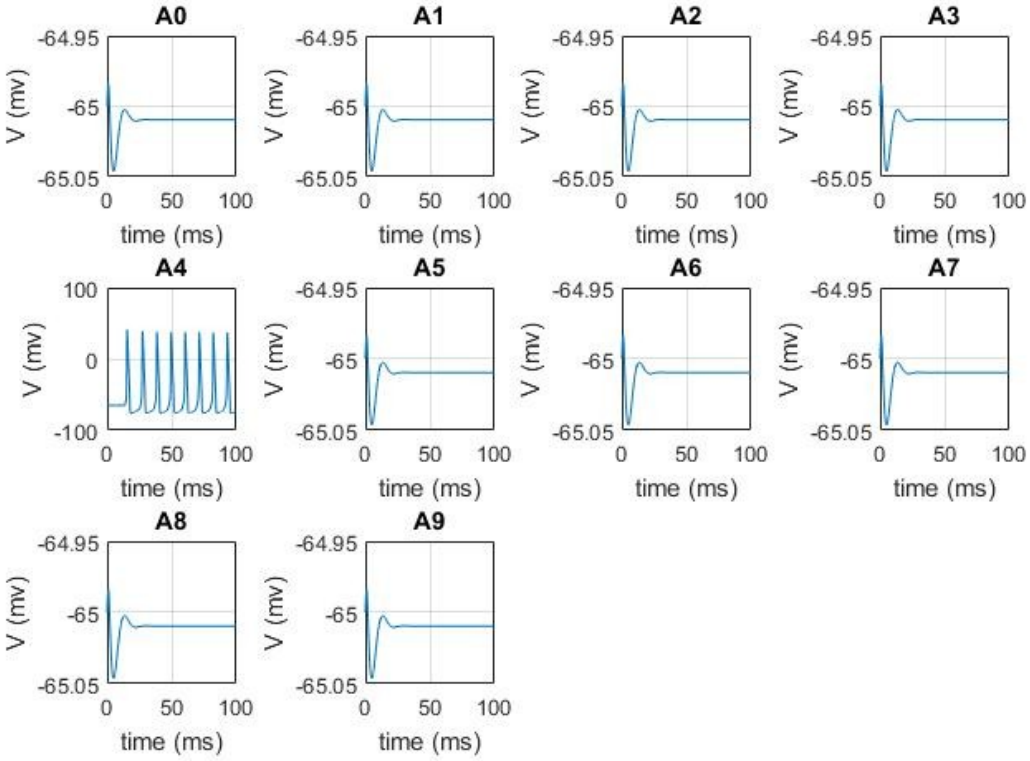

Figure 6. Operand A: Representation of number 4 in the brain with an array of 10 neuron flip-flops.

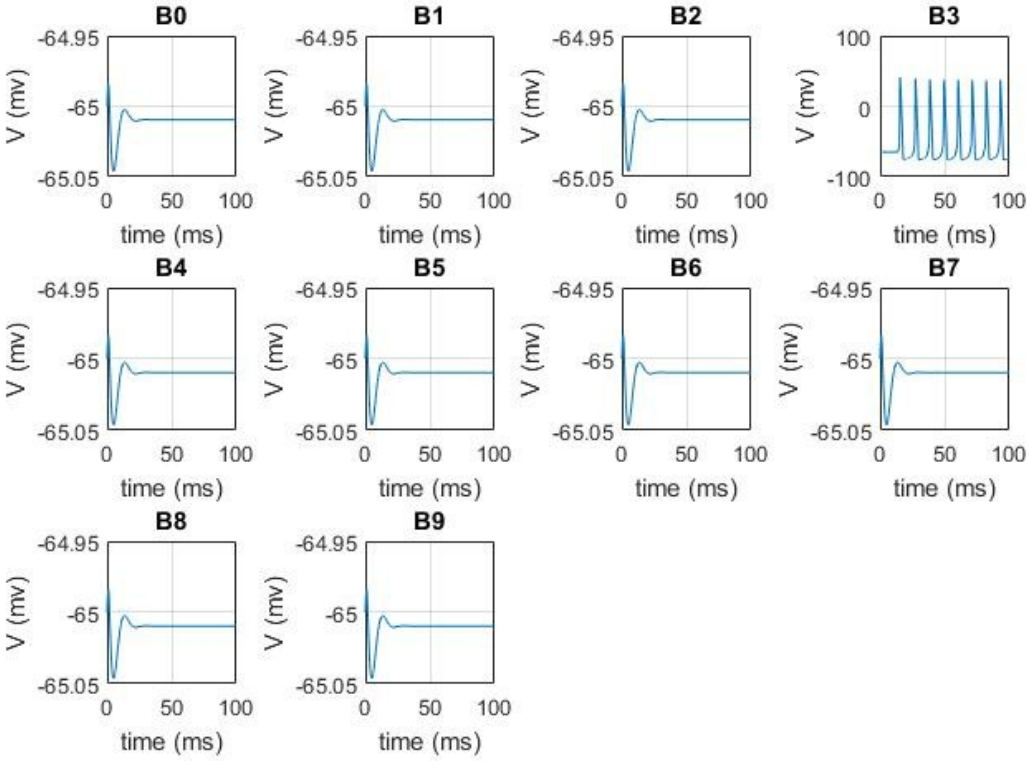

Figure 7. Operand B: Representation of number 3 in the brain with an array of 10 neuron flip-flops.

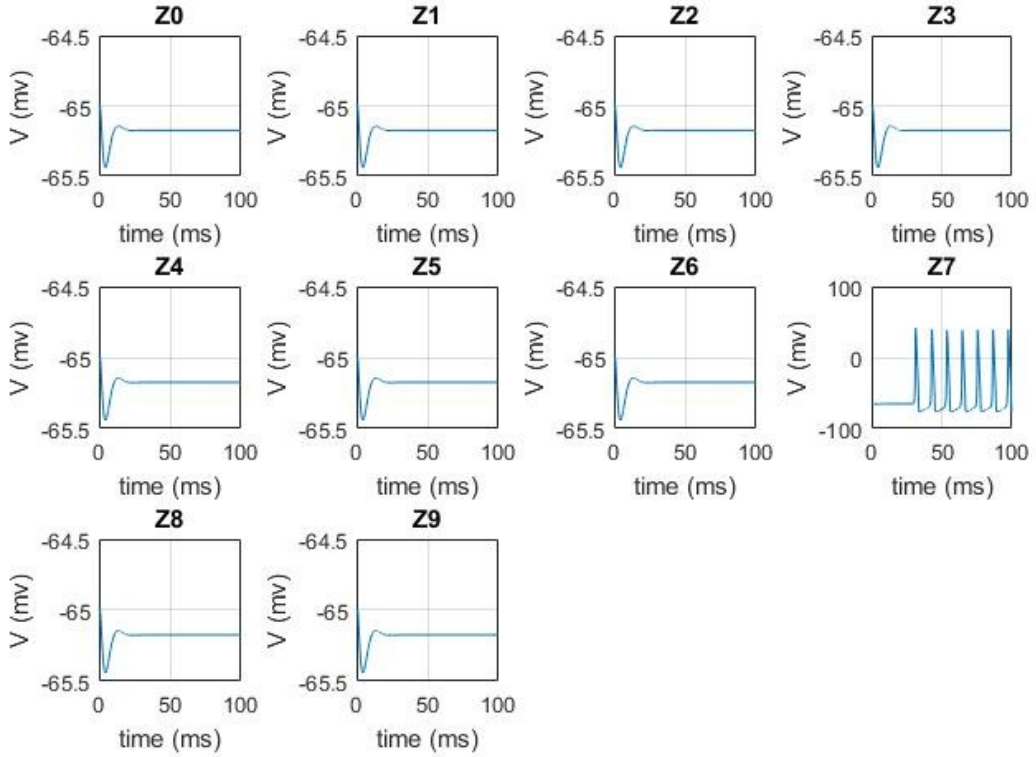

Figure 8. Resulting sum S: Representation of number 7, the sum of operands A and B, in the brain with an array of 10 neuron flip-flops.

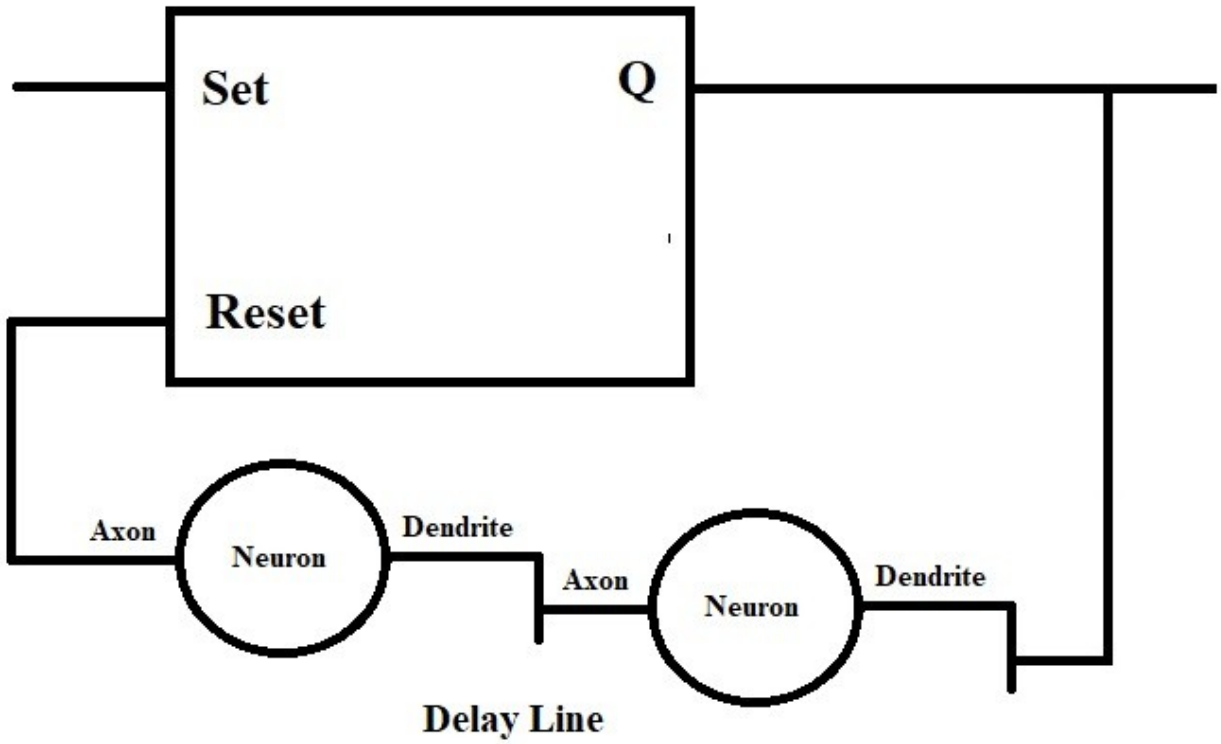

Figure 9. Monostable Circuit. The neuron flip-flop resets itself after a delay time. The delay line consists of several neurons connected in daisy chain.

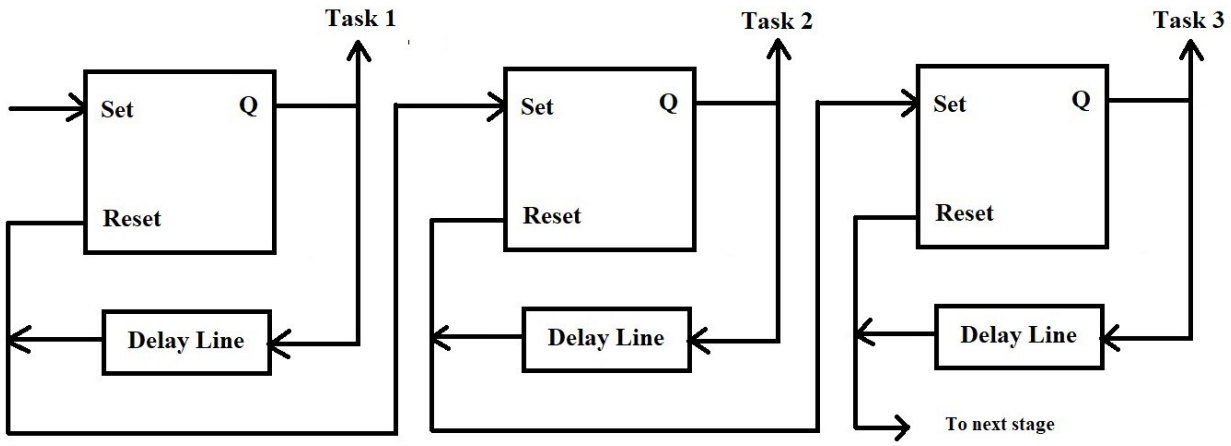

Figure 10. Task Sequencer Circuit

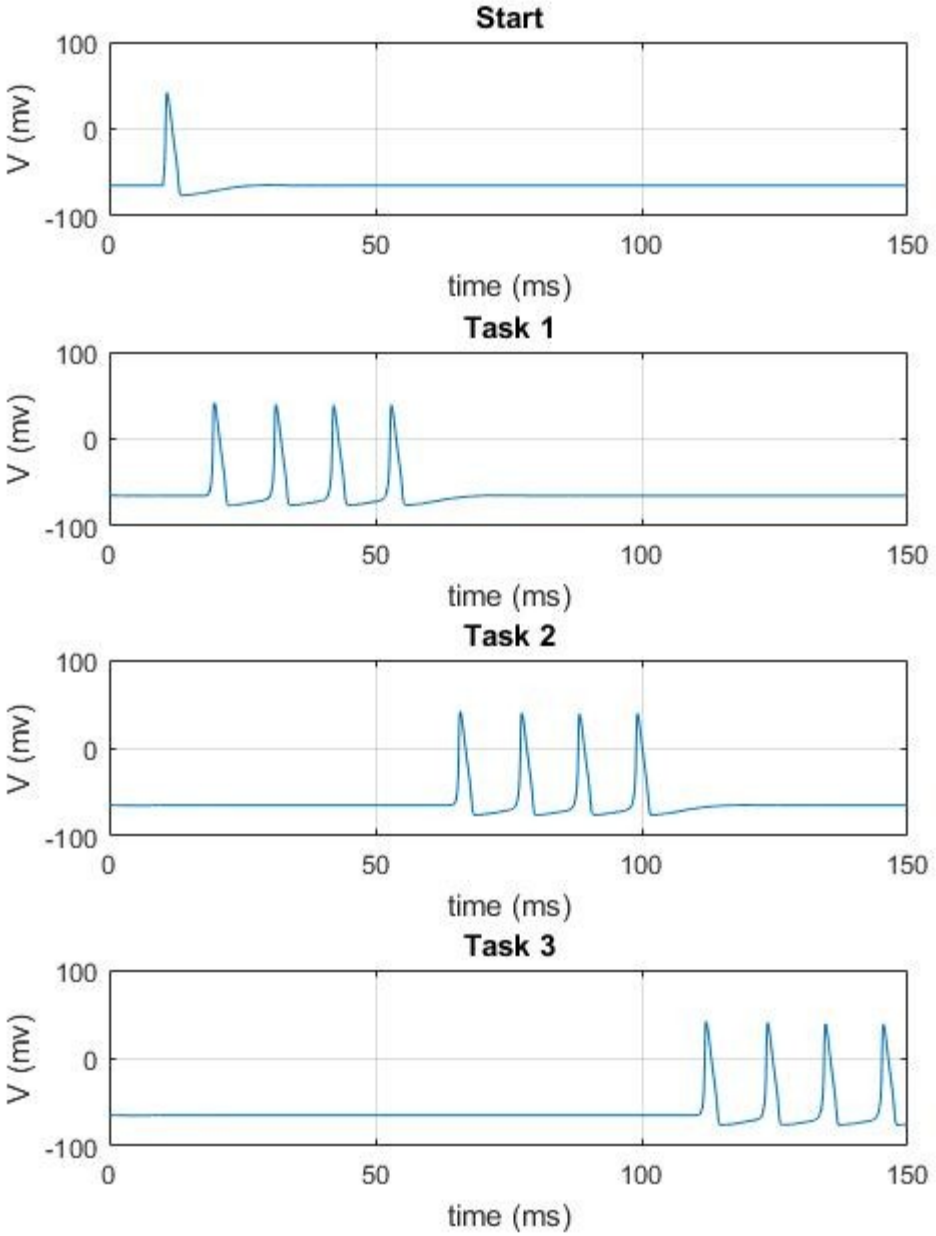

Figure 11. Sequencer Simulation.

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